

Application. No. : 10/022,297
Filing Date : December 12, 2001
Amendment Date : December 22, 2003
Office Action Date : September 25, 2003

REMARKS

Claims 1-32 were originally pending in the present application. Claims 27-32 were withdrawn in response to a restriction requirement and were subsequently cancelled. Claim 17 was canceled in response to a second Office Action. Claims 1, 5-12, 18, 23 and 24 are canceled herein. Claims 4, 13, 14, 16, 19 and 20 are amended herein. Claims 15, 21, 22, 25 and 26 remain pending as originally filed or as previously amended. Claims 33-37 are added herein. Accordingly, Claims 4, 13-16, 19-22, 25, 26 and 33-37 are presented herein for further consideration by the Examiner.

Response to Drawing Requirement (Checked Box 11 on the Office Action Summary)

Applicants note that Box 11 on the Office Action Summary is checked to indicate that the drawing correction filed on December 18, 2002, is approved by the Examiner and that corrected drawings are required in reply to the September 25, 2003 Office Action.

Applicants note that the same box was checked in the March 11, 2003 Office Action. In response to the March 11, 2003 Office Action, Applicants submitted the required corrected formal drawing by Certificate of Mail on June 10, 2003. The replacement formal drawing was submitted with a paper entitled *Submission of Replacement Formal Drawing Sheet*.

Applicants respectfully request the Examiner to acknowledge receipt of the replacement drawing sheet and to approve the replacement drawing sheet in the next communication to Applicants.

Response to the Objections of Claim 4

In the September 25, 2003 Office Action, the Examiner objects to Claim 4 because of informalities. In response the objection, Claim 4 is amended herein to clarify that the resin covers the solder and the chip as well as the land. In view of the amendments to Claim 4, Applicants respectfully request the Examiner to withdraw the objection to Claims 4 based on informalities.

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Response to the Rejection of Independent Claims 4 under 35 U.S.C. § 103(a)

In the September 25, 2003 Office Action, the Examiner rejects Claim 4 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,259,157 to Sakamoto. Applicants respectfully traverse the rejection of Claim 4 for following reasons.

Claim 4

Amended Claim 4 recites a semiconductor device comprising an aluminum substrate. A copper land is formed on the substrate. A semiconductor chip is mounted on the land. The semiconductor device further includes a solder layer only through which the semiconductor chip is joined with the land. The semiconductor device includes an epoxide synthetic resin that has a coefficient of expansion being generally less than approximately 23 ppm/°K (e.g., generally less than the coefficient of expansion of the aluminum substrate). The coefficient of expansion of the resin is generally greater than the coefficient of expansion of the copper land. The epoxide synthetic resin covers the land, the solder layer, and the semiconductor chip. The epoxide synthetic resin advantageously relieves the thermal stress on the solder layer. Thus, cracks in the solder layer or the semiconductor chips and the peeling of the semiconductor chips from the solder layer are effectively prevented without the conventional heat spreaders if the epoxide synthetic resin has a coefficient of expansion being generally less than approximately 23 ppm/°K. Additionally, no side walls are necessary if the epoxide is applied because the epoxide has sufficient viscosity. Further, the epoxide is also amenable to a reflow soldering method.

Sakamoto does not teach or suggest all the limitations of Claim 4. Specifically, Sakamoto does not disclose an epoxide synthetic resin having a coefficient of expansion that is generally less than approximately 23 ppm/°K (the coefficient of expansion of the aluminum substrate) and that is generally greater than the coefficient of expansion of the copper land. In contrast to the invention defined in Claim 4, Sakamoto discloses a thermosetting epoxy resin that covers an active element 8 mounted on a hybrid integrated substrate 1 having an aluminum substrate and a resin layer 5. Sakamoto teaches that the resin has the same coefficient of thermal expansion as the hybrid integrated circuit 1. (See, column 7 at lines 1-5, column 10 at lines 39-

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42, column 13 at lines 25-28 and Figures 1, 4 and 5 of Sakamoto.) Sakamoto further teaches that mismatch of thermal expansion coefficient between the resin and the active element 8 and the substrate 1 causes undesirable breakage in wires. (See, column 7 at lines 17-23 of Sakamoto.) Thus, Sakamoto teaches away from the invention defined in Claim 4 wherein the coefficient of expansion of the resin is different from the coefficient of expansion of the substrate.

Applicants respectfully disagree with the Examiner's statement that *the same material is utilized in Sakamoto as in Applicants' invention therefore it would have the same characteristics*. (See, page 3 of the September 25, 2003 Office Action.) The Examiner is disregarding the teaching of Sakamoto, because Sakamoto teaches a resin that has the same coefficient of thermal expansion as the hybrid integrated circuit. As discussed above, Claim 4 recites a particular relationship between the coefficients of expansion that is neither taught nor suggested in the art of record. The Examiner cannot pick and choose elements from the disclosure in the prior art and then use Applicants' claimed invention as a template for combining the elements in a manner not taught or suggested by the prior. Rather, *[t]here must be evidence that "a skilled artisan, confronted with the same problems as the inventors and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed."* See, *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); and *In re Werner Kotzab*, 217 F.3d 1365, 1371, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

For the reasons set forth above, Applicants respectfully submit that amended Claim 4 is not obvious in view of Sakamoto. Applicants further submit that Claim 4 is patentably distinguished over Sakamoto. Applicants respectfully request the Examiner to withdraw the rejection of Claim 4 under 35 U.S.C. § 103(a).

Response to the Rejection of Independent Claim 16 Under 35 U.S.C. § 103(a)

The Examiner rejects Claims 16 under 35 U.S.C. § 103(a) as obvious over Ueda (Japanese Publication No. 08-264674) in view of Yanagisawa (Japanese Patent No. 63213936).

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Claim 16

Claim 16 recites a semiconductor device comprising a substrate. A land is formed on the substrate. A semiconductor chip that controls electric power is mounted on the land. A solder layer joins the semiconductor chip with the land. The semiconductor chip is generally configured as a shape that has at least first and second corners positioned generally diagonally opposite to each other. The land has an outer boundary that defines at least first and second corner portions positioned in proximity to the first and second corners of the semiconductor chip. The outer boundary of the land further defines contiguous portions that extend next to the corner portions. The outer boundary at the contiguous portions is spaced apart from the semiconductor chip more than the outer boundary at the corner portions. The corner portions of the land generally confine the corners of the semiconductor chip therein. The area of the land is larger than an area of the semiconductor chip. The area of the land generally expands from the corners of the semiconductor chip such that the area of the land in the contiguous portions is greater than the area of the land in the first and second corner portions. As discussed in the specification, the increased area of the land in the contiguous portions enables bubbles in the paste of the solder to escape during the reflow solder process used to secure the semiconductor chip to the land.

Ueda does not teach or suggest all the limitations of Claim 16. Specifically, Ueda does not teach or suggest a semiconductor chip mounted to the land. Rather, in contrast to the invention defined in Claim 16, Ueda teaches a land 10 and a chip capacitor 8b mounted to the land 10. (See paragraph [0019] and Figures 2, 4, 6, 8 and 10 of Ueda.) The chip capacitor of Ueda does not correspond to the semiconductor chip defined in Claim 16.

In section 8 of the Office Action, the Examiner states that the semiconductor chip 1 is mounted on the land 10. Applicants respectfully disagree because Ueda teaches that the semiconductor chip 1 is mounted to the plate 7 so that heat can be radiated from the chip 1. (See paragraph [0003] of Ueda.) The chip mounted on the plate does not teach or suggest the chip mounted on the land as defined in Claim 16.

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Moreover, Ueda does not disclose the semiconductor chip defining at least two corners positioned generally diagonally opposite to each other, and does not disclose the land having the outer boundary defining at least two corner portions positioned in proximity to the corners of the semiconductor chip. In contrast, Ueda teaches the land 10 having a power supply layer 10a and an outgoing line of grand [*sic: ground*] layer 10b at opposite sides of the chip capacitor. (See paragraphs [0017] and [0019] and Figures 1-6 of Ueda.) In Figures 1-6 of Ueda, the power supply layer 10a and the outgoing line of grand [*sic: ground*] layer 10b appear to be aligned rectangular layers that are spaced apart. Furthermore, the land 10 and the chip 1 are on different portions of the Ueda device.

In addition to the foregoing differences, Ueda does not disclose contiguous portions extending next to the corner portions and spaced apart from the semiconductor chip by a greater distance than the corner portion is spaced apart from the semiconductor chip. Thus, Applicants respectfully submit that Claim 16 is not obvious in view of Sakamoto, and Applicants further submit that Claim 16 is patentably distinguished over Sakamoto. Applicants respectfully request the Examiner to withdraw the rejection of Claim 16 under 35 U.S.C. § 103(a).

Response to the Rejection of Dependent Claims

Claims 13-15 depend from Claim 4 and further define the invention defined in Claim 4. Claims 13-15 are patentably distinguished over the cited references for at least the reasons set forth above with respect to amended Claim 4, as well as for novel and nonobvious features recited therein.

Claims 19-22, 25 and 26 depend from Claim 16 and further define the invention defined in Claim 16. Claims 19-22, 25 and 26 are patentably distinguished over the cited references for at least the reasons set forth above with respect to amended Claim 16, as well as for novel and nonobvious features recited therein.

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Applicants respectfully submit that dependent Claims 13-15 and 19-22, 25 and 26 are allowable over the art of record, and Applicants respectfully request the Examiner to withdraw the rejection of Claims 13-15 and 19-22, 25 and 26 under 35 U.S.C. § 103(a).

New Claims 33-37

Applicants have added new method Claims 33-37 to define a method of manufacturing a semiconductor device generally in accordance with the apparatus defined in Claims 16, 19-22, 25 and 26. Applicants respectfully submit that new method Claims 33-37 should be examined along with apparatus Claims 16, 19-22, 25 and 26 in accordance with MPEP § 806.05(f). Applicants further submit that new Claims 33-37 are patentably distinguished over the art of record.

Summary

In view of the amendments to the claims and the foregoing remarks, Applicants respectfully request the Examiner to withdraw the rejections of 4, 13-16, and 19-22, 25 and 26. Applicants respectfully submit that Claims 4, 13-16, and 19-22, 25 and 26 are now in condition for allowance. Applicants further submit that new Claims 33-37 are also in condition for allowance. Applicants respectfully request the Examiner to pass this application to the issue process with Claims 4, 13-16, 19-22, 25, 26 and 33-37.

Applicants also respectfully request the Examiner to indicate approval of the replacement sheet of drawings submitted in response to the previous Office Action.

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Request for Telephone Interview

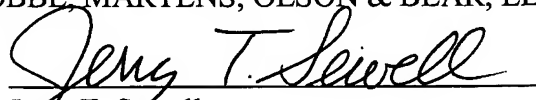
If there are any impediments to the prompt allowance of this application or if there are any questions or issues that may be resolved via a telephone interview, Applicants invite the Examiner to call the undersigned attorney of record at 949-721-2849 (direct) or at the general office telephone number listed below.

Dated: DECEMBER 23, 2003

Respectfully submitted,

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